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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,594	07/22/2004	Ching-Yu Tsai	MTKP0177USA	4593
27765	7590	06/17/2008	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			ZHAO, DAQUAN	
			ART UNIT	PAPER NUMBER
			2621	
			NOTIFICATION DATE	DELIVERY MODE
			06/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/710,594	TSAI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	DAQUAN ZHAO	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 05 May 2008.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-5, 11-17 and 23 is/are rejected.  
 7) Claim(s) 6-10 and 18-22 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 22 July 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/5/2008 has been entered.

### ***Response to Arguments***

2. Applicant's arguments filed 5/5/2008 have been fully considered but they are not persuasive.
3. Applicant argues, on pages 1-5 of the remark, the combination of Hoshi et al and Xue et al fail to teach the incoming bit-stream being a DV stream having data in frame (DIF) blocks; checking the incoming bit-stream for errors by checking the DIF blocks in the DV stream; The examiner disagrees.
4. Column 6, line 19- column 7 line 5 of Xue et al teach the CIP packet includes the DIF block DV data in the data field 28 and the data field 28 will occasionally be empty as a result of timing and/or source data availability considerations. Xue et al teach the problem when using the IEEE 1394, in column 2, lines 27-35, which is due to missing data in the CIP packet. column 2, line 66- column 3, line 29 of Xue et al teach checking if the incoming bit contains empty or non-empty CIP packet. Therefore the teaching of

Xue et al read on the incoming bit-stream being a DV stream having data in frame (DIF) blocks; checking the incoming bit-stream for errors by checking the DIF blocks in the DV stream;

5. For claim 12, applicant also argues, on pages 1-5 or the remark, the combination of Hoshi et al and Xue et al fail to teach "storing the video blocks and audio blocks in a memory". Hoshi et al teach in column 5, lines 10-18 a buffer storage (not shown) for storing the video and audio blocks.

6. For claim 1, applicant also argues, the combination of Hoshi et al, Xue et al and Ihara fail to teach "a memory coupled to the DV demuxer". Ihara teaches the memory 15 is couple to the demultiplexer 14 as shown in figure 2.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al (US 7,197,231 B2) and further in view of Xue et al (US 6,711,181 B1).
2. **In regards to claim 12,** Hoshi et al teach a method of storing digital video (DV) data, the method comprising the following steps: providing an interface module for

receiving an incoming signal and converting the incoming signal into an incoming bit-stream (e.g. figure 1, column 2, line 58- column 3, line 5); directly receiving the incoming bit-stream from the interface module (e.g. figure 1, column 5, lines 50-61); de-multiplexing received blocks in the incoming bit-stream into at least video blocks being in video sections and audio blocks being in audio sections (e.g. figure 1, lines 11-18, the TS is de-multiplexed into video and audio and output to the video decoder and audio decoder separately); and storing the video blocks and audio blocks in a memory (e.g. e.g. column 5, lines 11-18 and column 6, lines 19-27). However, Hoshi et al fail to teach checking the incoming bit-stream for error. Xue et al teach checking the incoming bit-stream for error (e.g. column 2, lines 9-36 and column 2, line 66- column 3, line 29, parsing the CIP header to a buffer, and determine if the CIP data is empty, Column 6, line 19- column 7 line 5 of Xue et al teach the CIP packet includes the DIF block DV data in the data field 28 and the data field 28 will occasionally be empty as a result of timing and/or source data availability considerations. Xue et al teach the problem when using the IEEE 1394, in column 2, lines 27-35, which is due to missing data in the CIP packet. column 2, line 66- column 3, line 29 of Xue et al teach checking if the incoming bit contains empty or non-empty CIP packet. Therefore the teaching of Xue et al read on the incoming bit-stream being a DV stream having data in frame (DIF) blocks; checking the incoming bit-stream for errors by checking the DIF blocks in the DV stream). It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Xue et al into the teaching of Hoshi et al to increase the reliability of the system.

**Regarding claim 13**, both Hoshi et al (e.g. column 2, lines 58-60) and Ihara (e.g. column 5, line 60) teach an IEEE 1394 interface.

3. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al (US 7,197, 231 B2) and Xue et al (US 6,711,181 B1) as applied to claim 12 above, and further in view of Ihara (US 7,199,891 B1).

See the teaching of Hoshi et al in claim 12 above.

**In regards to claim 1**, Hoshi et al also teach the incoming bit-stream is not buffered outside the interface module and the DV demuxer in column 5, lines 11-18. The de-multiplexer has a buffer storage inside. Hoshi et al fail to specify a memory coupled to the DV demuxer since buffer storage in the de-multiplexer is not shown. Ihara teaches a memory coupled to the DV demuxer (e.g. figure 2, memory 15 is coupled to the de-multiplexer 14, column 5, line 56- column 6, line 2). It would have been obvious for one ordinary skill in the art at the time the invention was made to incorporate the teaching of Ihara into the teaching of Hoshi et al to buffer the data after the is de-multiplexed because coupling two devices takes routine skill in the art, and it would have been obvious for one ordinary skill to try coupling the memory and the de-multiplexer since the number of options for connecting these two devices are limited (see KSR decision, rational E: “obvious to try”).

**Regarding claim 2**, both Hoshi et al (e.g. column 2, lines 58-60) and Ihara (e.g. column 5, line 60) teach an IEEE 1394 interface.

4. Claims 3, 4, 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al (US 7,197,231 B2), Xue et al (US 6,711,181 B1) and Ihara (US 7,199,891 B1) as applied to claims 1, 2 above, and further in view of Okamori (US 2003/0,053,486 A1) and Tan et al (US 5,959,684)

See the teaching of Hoshi et al and Ihara above.

**Regarding claim 3,** Hoshi et al, Xue et al and Ihara fail to teach manages a write block pointer and determines if the incoming bit-stream is compliant with a DV format. Okamori teaches determines if the incoming bit-stream is compliant with a DV format (e.g. paragraph [0061]). It would have been obvious to one ordinary skill in the art at the time the invention was made to determine if the incoming bit-stream is compliant with a DV format as taught by Okamori before de-multiplexing the data stream in the system of Hoshi et al and Ihara to reduce error and increase the reliability of the system.

Hoshi et al, Xue et al Ihara and Okamori fail to specify a write block pointer. Tan et al teach a write block pointer driven by the requirements of the de-multiplexing process (e.g. column 2, lines 30-36). It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Tan et al in to the system of Hoshi et al, Ihara and Okamori to increase the data processing speed for writing the data into a buffer after the de-multiplexing process.

**Regarding claim 4,** Xue et al teach extractor receiving the incoming bit-stream and checking the incoming bit-stream for error (e.g. column 2, lines 9-36 and column 2, line 66- column 3, line 29, parsing the CIP header to a buffer, and determine if the CIP data is empty). It would have been obvious to one ordinary skill in the art at the time the

invention was made to incorporate the teaching of Xue et al into the teaching of Hoshi et al, Ihara, Okamori and Tan et al to increase the reliability of the system.

**Regarding claim 5,** Xue et al teach the data extractor outputs received blocks of sections other than the video and audio sections to the host controller (column 2, line 66- column 3, line 29, parsing the CIP header to a buffer, and determine if the CIP data is empty).

**Regarding claim 11,** Tan et al teach storing the video and audio blocks in respective sections of the memory, the respective sections of the memory being determined according to the write block pointer; and storing the video and audio blocks within the respective sections according to a sequence number and a block number of each video and audio block in the incoming bit-stream (e.g. column 2, lines 23-45).

5. Claims 14, 16, 17, 15, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al (US 7,197,231 B2) and Xue et al (US 6,711,181 B1) as applied to claims 12,13 above, and further in view of Okamori (US 2003/0,053,486 A1) and Tan et al (US 5,959,684)

See the teaching of Hoshi et al above.

**Regarding claims 14 and 15,** Hoshi et al fail to teach manages a write block pointer and determine if the incoming bit-stream is compliant with a DV format. Okamori teaches determines if the incoming bit-stream is compliant with a DV format (e.g. paragraph [0061]). It would have been obvious to one ordinary skill in the art at the time the invention was made to determine if the incoming bit-stream is compliant with a DV

format as taught by Okamori before de-multiplexing the data stream in the system of Hoshi et al and Xue et al to reduce error and increase the reliability of the system.

Hoshi et al, Ihara and Okamori fail to specify a write block pointer. Tan et al teach a write block pointer driven by the requirements of the de-multiplexing process (e.g. column 2, lines 30-36). It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Tan et al in to the system of Hoshi et al, Xue et al and Okamori to increase the data processing speed for writing the data into a buffer after the de-multiplexing process.

**Regarding claim 16**, Xue et al teach extractor receiving the incoming bit-stream and checking the incoming bit-stream for error (e.g. column 2, lines 9-36 and column 2, line 66- column 3, line 29, parsing the CIP header to a buffer, and determine if the CIP data is empty). It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Xue et al into the teaching of Hoshi et al, Okamori and Tan et al to increase the reliability of the system.

**Regarding claim 17**, Xue et al teach the data extractor outputs received blocks of sections other than the video and audio sections to the host controller (column 2, line 66- column 3, line 29, parsing the CIP header to a buffer, and determine if the CIP data is empty).

**Regarding claim 23**, Tan et al teach storing the video and audio blocks in respective sections of the memory, the respective sections of the memory being determined according to the write block pointer; and storing the video and audio blocks

within the respective sections according to a sequence number and a block number of each video and audio block in the incoming bit-stream (e.g. column 2, lines 23-45).

***Allowable Subject Matter***

6. Claims 6-10 and 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daquan Zhao whose telephone number is (571) 270-1119. The examiner can normally be reached on M-Fri. 7:30 -5, alt Fri. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Thai Q, can be reached on (571)272-7382. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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